REMARKS

The Official Action mailed September 25, 2002, has been received and its contents carefully noted. Filed concurrently herewith is a *Request for Two Month Extension of Time*, which extends the shortened statutory period for response to February 25, 2003. Accordingly, Applicant respectfully submits that this response is being timely filed.

Applicant notes with appreciation the consideration of the Information Disclosure Statements filed on August 13, 2002; December 11, 1997, and February 7, 1996. However, Applicant has not received acknowledgement of the Information Disclosure Statement filed on December 28, 1999. Applicant respectfully requests that the Examiner provide a copy of the initialed Form PTO-1449 evidencing consideration of this Information Disclosure Statement with the following action.

Claims 1-59 are pending in the present application, of which claims 1, 5, 8, 9, 15, 19, 22, 23, 29, 31, and 36 are independent. Claims 1, 2, 4-29 and 36 have been amended. The Applicant notes with appreciation the allowance of claims 1-4, 6, 10, 14-18, 20, 21, 23-28, 44, 51 and 54. The Applicant further notes with appreciation the indication of the allowability of claims 7, 21, 33, 38, 41-43 and 45-47 (objected to as being dependent upon a rejected base claim). Accordingly, claims 1-59 are now pending in the present application and, for the reasons set forth in detail below, are believed to be in condition for allowance. Favorable reconsideration is requested.

Paragraph 4 of the Official Action rejects claims 5 and 19 as indefinite for failing to particularly point out and distinctly claims the subject matter which applicant regards as the invention. In response, the claims 5 and 19 have been amended to correct this informlaity and it is respectfully submitted that these claims are definite in light of the amendment.

Paragraph 6 of the Official Action rejects claims 5, 8, 19, 22, 29, 30, 48, 49, 52, 53, and 55 as obvious based on the combination of Japanese Patent 2-143152 to Koji and U.S. Patent No. 4,862,237 to Morozumi. The Applicants respectfully traverse the rejection because the Official Action has not made a *prima facie* case of obviousness.

As stated in MPEP §§ 2143-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or

motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." *In re Kotzab,* 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

The prior art, either alone or in combination, does not teach or suggest all the features of the independent claims. Independent claims 5, 8, 19, 22 and 29 recite an insulating substrate having a blocking layer. The Official Action concedes that Koji does not teach or disclose forming a blocking (silicon oxide) layer on the insulating substrate (p. 4, Paper No. 39). The Official Action cites Morozumi to show a silicon oxide film on an insulating substrate (p. 4, Paper No. 39). However, the Official Action has failed to show why the silicon oxide film of Morozumi would be applied to the insulating substrate of Koji. Since Koji and Morozumi do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained.

Furthermore, there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify Koji and Morozumi or to combine reference teachings to achieve the claimed invention. Koji teaches that the surface of the substrate corresponding to at least the i-region semiconductor layer is roughened and the relationship between the surface roughness (cm) and the crystal grain diameter (cm) is as follows: (surface roughness) × (crystal grain diameter) $\leq 10^{-5}$ (cm^2) in order to improve light absorption of a silicon film formed thereon (see English translation of Koji on p. 4, lines 3-15). Nothing in the

references themselves or in the knowledge generally available to one of ordinary skill in the art indicates why the Morozumi silicon oxide film would be applied to the Koji roughened surface of the substrate. Accordingly, the Applicant respectfully submits that there is no motivation to combine Morozumi's silicon oxide film on Koji's roughened surface of the substrate.

Also, independent claims 5 and 19 are amended so as to recite a device comprising a photoelectric conversion semiconductor device, an n-channel thin film transistor, and a p-channel thin film transistor over an insulating substrate having a blocking layer, wherein a semiconductor region of the photoelectric conversion semiconductor device and active layers of the n-channel and p-channel thin film transistors are formed from the same semiconductor layer on the blocking layer as shown in Figs. 1A-1F. It is respectfully submitted that Koji and Morozumi do not teach or suggest the features of claims 5 and 19, as amended.

In the present application, it is respectfully submitted that the prior art of record, alone or in combination, does not expressly or impliedly suggest the claimed invention and the Official Action has not presented a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.

Accordingly, reconsideration and withdrawal of the rejection of claims 5, 8, 19, 22, 29, 30, 48, 49, 52, 53, and 55 under 35 U.S.C. § 103(a) is in order and respectfully requested.

Paragraph 7 of the Official Action rejects claims 9, 11-13, 31, 32, 34-37, 39, 40, 50, and 56-59 as being unpatentable over Koji in view of Morozumi, and further in view of U.S. Patent No. 5,250,931 to Misawa et al.

Independent claims 9, 31, 36 also recite an insulating substrate having a blocking layer. Please incorporate the arguments above with respect to the deficiencies in Moji and Morozumi. Misawa does not cure the above-referenced deficiencies in Moji and Morozumi. Misawa is cited by the examiner in order to show that a semiconductor switch comprises complementary p-channel and n-channel thin film transistors. Misawa does not provide motivation to combine Morozumi's silicon oxide film with Koji's device as argued above. Moreover, since Misawa's device is used for driving an active matrix

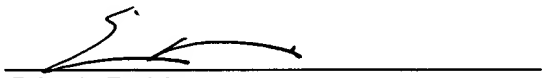
display panel, the Applicant respectfully submits that Misawa is not related to the claimed device comprising a photoelectric conversion semiconductor device. Also, there is no motivation to combine Misawa's n-channel and p-channel transistors with Morozumi's silicon oxide film and Koji's device.

Further, independent claims 9 and 31 recite the feature that a Raman spectrum of the semiconductor layer exhibits a peak deviated from that which stands for a single crystal for the semiconductor. The Official Action broadly asserts that Fig. 3G of Koji teaches this feature of the invention. The Applicant respectfully disagrees and submits that this feature of the present invention is not taught or suggested by Koji, Morozumi, or Misawa, either alone or in combination.

Accordingly, reconsideration and withdrawal of the rejection of claims 9, 11-13, 31, 32, 34-37, 39, 40, 50, and 56-59 under 35 U.S.C. § 103(a) is in order and respectfully requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number listed below.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend claims 1, 2, 4-29, and 36 as follows:

1. (Amended) A device for sensing a light comprising:

a light sensor region and a semiconductor switch region adjacent to and operatively connected with said light sensor region over an insulating substrate having a blocking layer,

wherein a semiconductor region of the light sensor region and an active region of the semiconductor switch comprise the same semiconductor layer, the semiconductor layer having a semi-amorphous structure formed on [a] the blocking layer over the insulating substrate, and

wherein a Raman spectrum of the semiconductor layer exhibits a peak deviated from that which stands for a single crystal for the semiconductor.

2. (Amended) [The] A device [of] according to claim 1, wherein said semiconductor layer comprises hydrogen doped silicon.

4. (Amended) [The] A device [of] according to claim 1, wherein said light sensor region comprises at least two semiconductor regions having different electrical properties and forming a junction.

5. (Amended) A device for sensing a light comprising a photoelectric conversion semiconductor device, an n-channel thin film transistor, and a p-channel thin film transistor over an insulating substrate having a blocking layer, the device produced by a process comprising the steps of:

forming [a] the blocking layer on [an] the insulating substrate;

depositing a semiconductor layer on the blocking layer;

[forming a photoelectric conversion semiconductor device on said substrate, a semiconductor region of the photoelectric conversion semiconductor device comprising a p-type impurity semiconductor region, an intrinsic semiconductor region, and an n-type impurity semiconductor region; and

forming an n-channel thin film transistor for driving the photoelectric conversion semiconductor device over the substrate, an active layer of the thin film transistor comprises a source region, a drain region, and a channel region;

wherein said semiconductor regions are arranged in order with said p-type impurity semiconductor region adjacent said intrinsic semiconductor region and said intrinsic semiconductor region adjacent said n-type impurity semiconductor region in said photoelectric conversion semiconductor device, said order being in a direction perpendicular to that in which a light to be sensed is incident thereon, and

wherein the semiconductor region of the photoelectric conversion semiconductor device and the active layer of the thin film transistor comprises the same semiconductor layer]

forming at least first, second, and third semiconductor islands by patterning the semiconductor layer;

forming first, second, and third conductive layers over the first, second, and third semiconductor islands with an insulating film interposed therebetween, respectively;

adding p-type impurities to the first semiconductor island and a first portion of the third semiconductor island by using the first and third conductive layers as masks; and

adding n-type impurities to the second semiconductor island and a second portion of the third semiconductor island by using the second and third conductive layers as masks.

6. (Amended) [The] A device [of] according to claim 1, wherein the semiconductor layer has lattice distortion and the peak of a laser Raman spectrum of the semiconductor layer is shifted to a lower wave number than $520cm^{-1}$.

7. (Amended) [The] A device [of] according to claim 5, wherein the semiconductor layer has lattice distortion and the peak of a laser Raman spectrum of the semiconductor layer is shifted to a lower wave number than $520cm^{-1}$.

8. (Amended) A device for sensing a light comprising:

a light sensor region and a semiconductor switch region adjacent to and operatively connected with said light sensor region over an insulating substrate having a blocking layer,

wherein a semiconductor region of the light sensor region and an active region of the semiconductor switch region comprise the same semiconductor layer formed on [a] the blocking layer located on the insulating substrate, and

wherein said semiconductor layer has at least one of and electron mobility in a range of 15[-] to 300 $cm^2/Vsec$ and a hole mobility in a range of 10[-] to 200 $cm^2/Vsec$.

9. (Amended) A device for sensing a light comprising:

a light sensor region and [a] n-type and p-type semiconductor switch regions adjacent to and operatively connected with said light sensor region over an insulating substrate having a blocking layer,

wherein a semiconductor region of the light sensor region and [an] active regions of the n-type and p-type semiconductor switch regions comprise the same semiconductor layer formed on [a] the blocking layer located on the insulating substrate, and

wherein a Raman spectrum of the semiconductor layer exhibits a peak deviated from that which stands for a single crystal for the semiconductor[, and said semiconductor switch region comprises complementary p-channel and n-channel thin film transistors].

10. (Amended) [The] A device [of] according to claim 9, wherein said semiconductor layer comprises hydrogen doped silicon.

11. (Amended) [The] A device [of] according to claim 9, wherein said light sensor region comprises at least two semiconductor regions having different electrical properties and forming a junction.

12. (Amended) [The] A device [of] according to claim 11, wherein said two semiconductor regions in said light sensor region are arranged in a lateral direction on said substrate.

13. (Amended) [The] A device [of] according to claim 9, wherein said semiconductor layer has at least one of an electron mobility in a range from 15 to 300 $cm^2/Vsec$ and a hole mobility in a range from 10 to 200 $cm^2/Vsec$.

14. (Amended) [The] A device [of] according to claim 1, wherein said semiconductor layer has at least one of an electron mobility in a range from 15 to 300 $cm^2/Vsec$ and a hole mobility in a range from 10 to 200 $cm^2/Vsec$.

15. (Amended) A device for reading an image comprising:

an image sensor region and a semiconductor switch region adjacent to and operatively connected with said image sensor region over an insulating substrate having a blocking layer,

wherein a semiconductor region of the light sensor region and an active region of the semiconductor switch region comprise the same semiconductor layer formed on [a] the blocking layer located on the insulating substrate, and

wherein said semiconductor layer has a semi-amorphous structure comprising a mixture of amorphous and crystalline structures, in which a Raman spectrum of the semiconductor film exhibits a peak deviated from that which stands for a single crystal of the semiconductor.

16. (Amended) [The] A device [of] according to claim 15 wherein said semiconductor layer comprises hydrogen doped silicon.

17. (Amended) [The] A device [of] according to claim 15 wherein said semiconductor switch region comprises a thin film transistor of which the active region is formed of said semiconductor layer.

18. (Amended) [The] A device [of] according to claim 15 wherein said image sensor region comprises at least two semiconductor regions having different electrical properties and forming a junction.

19. (Amended) A device for reading an image produced by a process comprising the steps of:

forming a blocking layer on an insulating substrate;

depositing a semiconductor layer on the blocking layer;

[forming a photoelectric conversion semiconductor device on said substrate, a semiconductor region of said photoelectric conversion semiconductor device comprising a p-type impurity semiconductor region, an intrinsic semiconductor region, and an n-type impurity semiconductor region; and

forming a thin film transistor on said substrate, an active region of the thin film transistor comprising a source region, a drain region, and a channel region,

wherein the semiconductor region of said photoelectric conversion semiconductor device and the active region of the thin film transistor comprise the same semiconductor layer, and

wherein said semiconductor regions are arranged in order with said p-type impurity semiconductor region adjacent said intrinsic semiconductor region and said intrinsic semiconductor region adjacent said n-type impurity semiconductor region in said photoelectric conversion semiconductor device, said order being in a direction perpendicular to that in which an image to be read is incident thereon]

forming at least first, second, and third semiconductor islands by patterning the semiconductor layer;

forming first, second, and third conductive layers over the first, second, and third semiconductor islands with an insulating film interposed therebetween, respectively;

adding p-type impurities to the first semiconductor island and a first portion of the third semiconductor island by using the first and third conductive layers as masks; and

adding n-type impurities to the second semiconductor island and a second portion of the third semiconductor island by using the second and third conductive layers as masks,

wherein the third semiconductor islands has a p-type impurity semiconductor region adjacent an intrinsic semiconductor region and an n-type impurity semiconductor region adjacent the intrinsic semiconductor region in order in a direction perpendicular to that in which an image to be read is incident thereon.

20. (Amended) [The] A device [of] according to claim 15 wherein the semiconductor layer has lattice distortion and the peak of a laser Raman spectrum of the semiconductor layer is shifted to a lower wave number than $520cm^{-1}$.

21. (Amended) [The] A device [of] according to claim 19 wherein the semiconductor layer has lattice distortion and the peak of a laser Raman spectrum of the semiconductor layer is shifted to a lower wave number than $520cm^{-1}$.

22. (Amended) A device for reading an image comprising:

an image sensor region and a semiconductor switch region adjacent to said operatively connected with said image sensor region over an insulating substrate having a blocking layer,

wherein a semiconductor region of the light sensor region and an active region of the semiconductor switch region comprise the same semiconductor layer formed on [a] the blocking layer located on the insulating substrate, and

wherein said semiconductor layer has at least one of an electron mobility in a range of 15[-] to 300 cm^2/Vsec and a hole mobility in a range of 10[-] to 200 cm^2/Vsec.

23. (Amended) A device for reading an image comprising:

an image sensor and a semiconductor switch region adjacent to and operatively connected with said image sensor region over an insulating substrate having a blocking layer,

wherein a semiconductor region of the light sensor region and an active region of the semiconductor switch region comprise the same semiconductor layer formed on [a] the blocking layer located on the insulating substrate, and

wherein said semiconductor layer has a semi-amorphous structure in which a Raman spectrum of the semiconductor film exhibits a peak deviated from that which stand for a single crystal of the semiconductor, and said semiconductor switch region comprises complementary p-channel and n-channel thin film transistors.

24. (Amended) [The] A device [of] according to claim 23 wherein said semiconductor layer comprises hydrogen doped silicon.

25. (Amended) [The] A device [of] according to claim 23 wherein said image sensor region comprises at least two semiconductor regions having different electrical properties and forming a junction.

26. (Amended) [The] A device [of] according to claim 25 wherein said two semiconductor regions in said image sensor region are arranged in a lateral direction on said substrate.

27. (Amended) [The] A device [of] according to claim 23 wherein said semiconductor layer has at least one of an electron mobility in a range from 15 to 300 cm^2/Vsec and a hole mobility in a range from 10 to 200 cm^2/Vsec.

28. (Amended) [The] A device [of] according to claim 15 wherein said semiconductor layer has at least one of an electron mobility in a range from 15 to 300 $cm^2/Vsec$ and a hole mobility in a range from 10 to 200 $cm^2/Vsec$.

29. (Amended) A device for sensing a light comprising:

a light sensor region and a semiconductor switch region adjacent to and operatively connected with said light sensor region over an insulating substrate having a blocking layer,,

wherein a semiconductor region of the light sensor region and an active region of the semiconductor switch region comprise the same semiconductor layer formed on [a] the blocking layer located on the insulating substrate, and

wherein said semiconductor layer has at least one of an electron mobility greater than 15 $cm^2/Vsec$ and a hole mobility greater than 10 $cm^2/Vsec$.

36. (Amended) A device comprising:

an insulating substrate;

a blocking layer on said insulating substrate;

first, second, and third semiconductor islands on said blocking layer;

p-type impurity regions in said first semiconductor island with a first channel region interposed therebetween and in a first region of said third semiconductor island;

n-type impurity regions in said second semiconductor island with a second channel region and in a second region of said third semiconductor island;

an insulating film on said first, second, and third semiconductor islands; and

first and second gate electrodes over said first and second channel regions, respectively, with said insulating film interposed therebetween,

wherein a Raman spectrum of each of said first, second, and third semiconductor islands exhibits a peak deviated from that which stands for a single crystal of the semiconductor, and

wherein said first semiconductor island has a mobility of 10[-] to 300 cm^2/Vsec and said second semiconductor island has a mobility of 15[-] to 300 cm^2/Vsec.